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EEL 4744L: Microprocessor Applications Laboratory

Lab 6: Logic State Analysis of the MC68HC11 Bus

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**Objective**

The object of this lab is to understand the timing of bus cycles and the operation of the MC68HC11 in expanded mode.

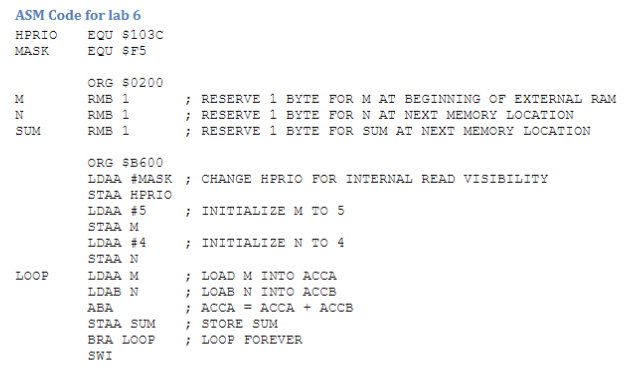
**Introduction/Background/Theory**

To make the HC11 more efficient, its developers created a way to reduce the number of pins required for reading and writing to memory. The processor has sixteen pins that are used to read and write from AD15-AD8 and AD7-AD0. During the first half of an E-clock cycle, the processor is required to access an address in memory and the AS (address strobe) signal drives the lower order pins (A7-A0). After the first half of the cycle, those same low order pins (D7-D0), are used to read and write data.

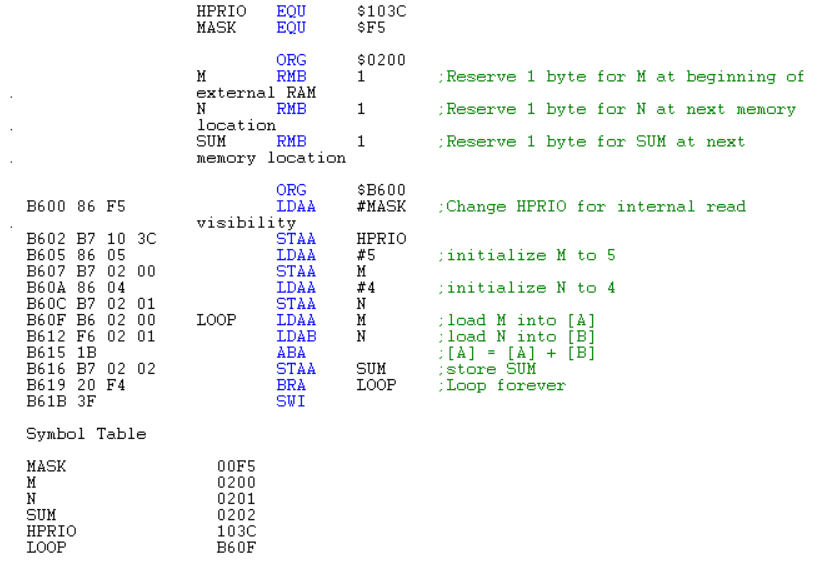
Being able to multiplex those pins for use as either an address bus or data bus cuts down on the overhead of having more pins to do the same job. This lab will show the relation of signals moving across pins such as AD15-AD8, AD7-AD0, the E-clock, AS, and R/W\* and how they all work together to execute a set of instructions.

**Procedure**

1. The lab required downloading the following ASM code, shown in Fig 1., to the HC11. A list file was also to be created showing the steps performed by the processor at each cycle (Fig 2.).

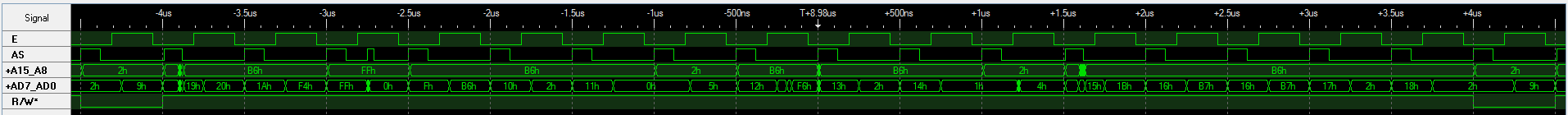


**Figure 1**: Assembly language code showcasing the infinite loop required for analysis



**Figure 2**: List file created after compiling the above ASM code.

2. During the lab, a logic analyzer was provided to connect to the HC11 and produce a time chart illustrating the operations occurring at pins AD15-A8 and AD7-AD0, as well as the E-clock, R/W\*, and AS pins. Below, Fig3. shows the values of each of the signals during a single loop of the branching instructions shown in Fig. 1.



**Figure 3**: A screen capture of the logic analyzer showing the values of the requested pins during a single loop

**Conclusions**

This lab was not inherently difficult, as it was mostly analysis of data. It was interesting to see the individual steps the HC11 takes to complete an assigned job.

**Questions**

1. Cycle-by-cycle execution table

|  |  |  |  |
| --- | --- | --- | --- |
| Cycle | Address | Data | R/W\* |
| 1 | B600 | 86 | 1 |
| 2 | B601 | F5 | 1 |
| 3 | B602 | B7 | 1 |
| 4 | B603 | 10 | 1 |
| 5 | B604 | 3C | 0 |
| 6 | B605 | 86 | 1 |
| 7 | B606 | 05 | 1 |
| 8 | B607 | B7 | 1 |
| 9 | B608 | 02 | 1 |
| 10 | B609 | 00 | 0 |
| 11 | B60A | 86 | 1 |
| 12 | B60B | 04 | 1 |
| 13 | B60C | B7 | 1 |
| 14 | B60D | 02 | 1 |
| 15 | B60E | 01 | 0 |
| 16 | B60F | B6 | 1 |
| 17 | B610 | 02 | 1 |
| 18 | B611 | 00 | 1 |
| 19 | B612 | F6 | 1 |
| 20 | B613 | 02 | 1 |
| 21 | B614 | 01 | 1 |
| 22 | B615 | 1B | 1 |
| 23 | B616 | B7 | 1 |
| 24 | B617 | 02 | 1 |
| 25 | B618 | 02 | 0 |
| 26 | B619 | 20 | 1 |
| 27 | B61A | F4 | 1 |
| 28 | B61B | 3F\* | 1 |

\*SWI is listed as taking 14 cycles to complete; however, the data bus is not essential after the first cycle.

2. The IRV bit is primarily used in expanded or special test modes as it is used in the debugging process of using a logic analyzer. It is tied to the E clock and is low when SMOD is low but high when SMOD is high.

3. During a cycle, when AS is 1, the AD7-AD0 bus lines start with an address and then alternate to data when AS is 0. For example, when the PC reaches address B619 and AS is 1, AD15-AD8 reads B6 while AD7-AD0 reads 19 followed by 20 when AS is 0.

4. The HC11 conducts a read cycle when the signal at R/W\* is 1 and conducts a write cycle when the signal at R/W\* is 0.